Code No: 114DN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE, BME)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A **(25 Marks)**

1.a)	Define rise time.	[2M]
b)	Draw and briefly explain the RC differentiator circuit.	[3M]
c)	What is meant by clipping in wave shaping?	[2M]
d)	Explain Clipping at two independent levels with circuit.	[3M]
e)	Compare unidirectional and bi-directional Sampling Gates.	[2M]
f)	Draw the Piecewise Linear Diode Characteristics.	[3M]
g)	Write a basic principle of time base generator.	[2M]
h)	Write the Methods of Generating Time Base Waveform.	[3M]
i)	Define positive and negative logic systems.	[2M]
j)	List out the applications of sweep circuits.	[3M]

Part-B **(50 Marks)**

2. Draw the output of the low pass RC circuit for different time constant to
a) Pulse input.
b) Step voltage input. [5+5]

OR

3.a) Prove that for any periodic input waveform the average level of the steady state output signal from RC high pass circuit is always zero.
b) Draw and explain the response of RLC circuit for step input. [5+5]

4. Classify different types of clipper circuits. Draw their circuits and explain their operation and also transfer characteristics. [10]

OR

5.a) State and prove clamping circuit theorem.
b) Explain negative peak clipper with and without reference voltage. [5+5]

6.a) Explain the operation of linear bidirectional sampling gate using transistors.
b) Explain in detail the junction diode switching times. [5+5]

OR

7.a) Explain about basic operation principles of sampling gates.
b) Write the advantages and disadvantages of unidirectional diode gate. [5+5]

8. Explain with neat diagram the following methods of linearizing a voltage sweep.
   a) Miller Sweep
   b) Bootstrap weep.
   Compare their merits and limitations. [5+5]

OR

9. Draw and explain the working principle of bistable multivibrator circuit and also explain the merits and limitations of it. [10]

10.a) Explain about DTL NAND gate.
   b) Distinguish between voltage and current sweep circuit. [4+6]

OR

11. Draw the circuit of a linear current sweep and explain its operation with wave forms. Explain the necessity of generating trapezoidal wave form. [10]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2016
PULSE AND DIGITAL CIRCUITS
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

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Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A **(25 Marks)**

1.a) Why does resistive attenuator need to be compensated. [2]
b) Derive an expression for the output of a high-pass circuit excited by a ramp input. [3]
c) Draw the basic circuit diagram of negative peak clamper circuit. [2]
d) Explain the working of an emitter coupled clipper. [3]
e) Explain the effect of pedestal in gate circuit. [2]
f) Explain the variation of saturation parameters of transistor with temperature? [3]
g) Define UTP and LTP. [2]
h) Write the difference between current time base generator and voltage time base generators. [3]
i) Draw the diagram of OR gate using diodes. [2]
j) Explain the principle of synchronization. [3]

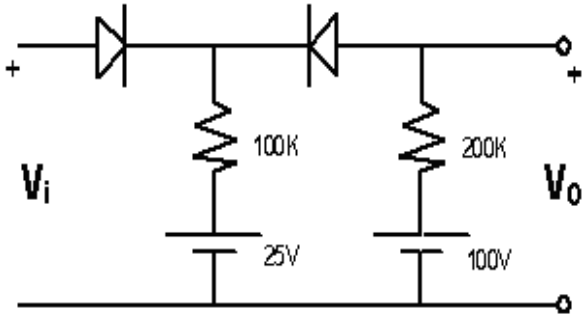
PART - B **(50 Marks)**

2.a) A symmetrical square wave whose peak-to-peak amplitude is 8V and whose average value is zero is applied to an RC integrating circuit. The time constant is equal to half -period of the square wave. Find the peak to peak value of the output amplitude.
b) Explain the working of high-pass RC circuit as a differentiator. [5+5]

OR

3.a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.
b) Draw the response of the circuit for step input critically damped and over damped cases for a fixed value of R and C. [5+5]

4.a) For the circuit shown in figure, an input voltage V_i linearly varies from 0 to 120 V is applied. Sketch the output voltage V_o to the same time scale. (Assume ideal diodes).



b) State and prove the clamping circuit theorem. [5+5]

OR

5.a) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [7+3]

6.a) Write a short note on switching times of a transistor.

b) With the neat circuit diagram, explain the operation of unidirectional sampling gate for multiple inputs. [5+5]

OR

7.a) Discuss in detail about breakdown voltages of a transistor.

b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [5+5]

8.a) With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled monostable multivibrator.

b) Explain how the deviation from linearity is expressed in terms of errors. [6+4]

OR

9.a) With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator.

b) What is hysteresis? Explain how hysteresis can be eliminated in a Schmitt trigger? [6+4]

10.a) Explain working of monostable relaxation device as a divider.

b) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL NAND gate with this. [5+5]

OR

11.a) What is phase jitter? How to reduce it in frequency division?

b) Draw and explain a diode AND circuit for negative logic and how it works. And how an OR circuit acts as a buffer circuit? [5+5]

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Code No: 114DN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, October/November - 2016
PULSE AND DIGITAL CIRCUITS
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART - A **(25 Marks)**

1.a)	What do you mean by linear network?	[2]
b)	Why RC circuits are commonly used compared to RL circuits.	[3]
c)	Distinguish between comparators and clipping circuits.	[2]
d)	What do you mean by double ended clipper?	[3]
e)	How does diode acts as a switch?	[2]
f)	What do you mean by turn ON time of a transistor?	[3]
g)	What are the applications of Schmitt trigger?	[2]
h)	What are the applications of time-base generators?	[3]
i)	What do you mean by synchronization?	[2]
j)	Name the technologies which use bipolar transistors.	[3]

PART - B **(50 Marks)**

2.a) Prove that for any periodic input waveform the average level of the steady state output signal from the RC high pass circuit is always zero.
b) Derive an expression for the rise time of the output of a low pass RC circuit excited by a step input. [5+5]

OR

3.a) Prove that a low pass RC circuit with a large time constant acts as an integrator.
b) Derive the expression for percentage tilt of a square wave output of RC high pass circuit. [5+5]

4.a) Draw the basic circuit diagram of negative peak clamper circuit and explain its operation.
b) With help of a neat circuit diagram explain the working of a two – level diode clipper. [5+5]

OR

5.a) State and prove clamping circuit theorem.
b) Write short notes on transistor clippers. [5+5]

6.a) Explain the operation of transistor switch in saturation.

b) For a common emitter amplifier, V_{cc} = 15V, R_c = 1.5kΩ and I_B = 0.3 mA. Determine the value of $h_{FE(min)}$ for saturation to occur, if R_c is changed to 500 Ω will the transistor be saturated. [5+5]

OR

7.a) With the help of a neat circuit diagram and waveforms, explain the operation of Four diode sampling gate.

b) With the help of a neat circuit diagram and waveforms, explain the operation of Six diode sampling gate. [5+5]

8.a) Explain the operation of fixed-bias binary with a triggering circuit and waveforms.

b) Design a Schmitt trigger circuit to have UTP=6V and LTP=3V using silicon Transistor Whose $h_{FE(min)}$=40. Assume necessary data. [5+5]

OR

9.a) Draw the circuit diagram of Bootstrap time base generator and explain its operation with necessary waveforms.

b) Compare the voltage and current time base generators with some examples. [5+5]

10.a) Illustrate the terms synchronization and frequency division of a sweep generator.

b) With the help of neat waveforms explain sine wave frequency division with a sweep circuit. [5+5]

OR

11.a) With a neat circuit diagram explain the operation of a TTL tristate output.

b) With the help of neat circuit diagram and truth table explain

(i) RTL OR gate

(ii) RTL AND gate. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2017
PULSE AND DIGITAL CIRCUITS
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

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Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Obtain the response of high pass RC circuit for a ramp input. [2]
b) Define % tilt of RC circuit. [3]
c) Write the applications of voltage comparator. [2]
d) Draw Negative biased Negative clipper circuit. [3]
e) Draw the piecewise linear diode characteristics. [2]
f) When transistor acts as a switch? [3]
g) Define multivibrator. [2]
h) Compare different multivibrators. [3]
i) Explain the frequency division in the sweep circuit. [2]
j) Define positive and negative logic systems. [3]

PART-B

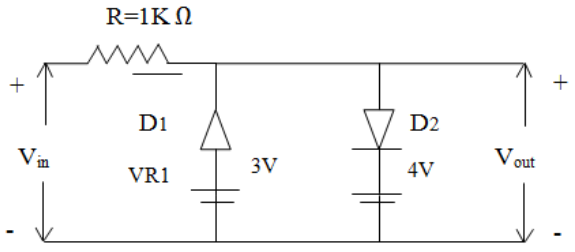
(50 Marks)

2. Draw the output of the low pass RC circuit for different time constant to:
a) Pulse input b) Step input. [10]

OR

3.a) Derive the expression for percentage tilt for a square wave output of RC high pass circuit.
b) A symmetrical square wave whose peak to peak amplitude is 2μ and whose average value in zero is applied to an RC integrator circuit. The time constant is equal to half the period of square wave, find the peak to peak value of output amplitude. [6+4]

4.a) Draw the circuit diagram of a DC restorer circuit with and without reference voltage and explain its operation for a sinusoidal input signal.
b) Explain the operation of the following double diode clipper and sketch the output wave form for a sinusoidal input shown in figure. [5+5]



OR

5.a) State and prove clamping circuit theorem.
b) Explain negative peak clipper with and without reference voltage. [5+5]

6.a) Explain the operation of linear bidirectional sampling gate using transistor.

b) Explain in detail the junction diode switching times. [6+4]

OR

7.a) Explain with relevant diagram the various transistor switching times.

b) For a CE circuit V_{CC} = 10V, R_C= 1K Ω IB =0.2A. Determine

i) The value of $h_{fe(min)}$ for saturation to occur.

ii) If R_C is change to 220Ω, will the transistor be saturated? [5+5]

8.a) Draw the circuit of a self biased transistor binary and develop the design and steps of analysis.

b) For a mono stable vibrator calculate the input pulse width for the design values of R_C = 2k Ω R_B = 10K Ω C = 0.1 μ F, V_{CC} = 10V and V_{BE}(Sat) = 0.8V. [5+5]

OR

9. Draw and explain the working principle of astable multivibrator circuit and also explain the merits and limitations of it. And also derive the expression for its pulse width. [10]

10. Discuss in detail the sine wave frequency division with a sweep circuit. [10]

OR

11. Draw and explain 2-input NAND gate with functional table. [10]

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Code No: 124CV **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2018
ELECTRONIC CIRCUIT ANALYSIS
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) How the amplifiers are classified? [2]
b) State and prove Miller's theorem. [3]
c) What is gain bandwidth product? [2]
d) Why emitter bypass capacitor is needed? [3]
e) How the stability of amplifier will affect by negative feedback amplifier? [2]
f) State the necessary conditions for oscillator. [3]
g) Define conversion efficiency of power amplifiers. [2]
h) How is crossover distortion eliminated in class AB amplifier? [3]
i) What are the applications of tuned amplifier? [2]
j) What is the coefficient coupling in a double tuned amplifier? [3]

PART-B

(50 Marks)

2.a) Draw the equivalent circuit for the CE and CC configurations subject to the restriction that $R_L = 0$. Show that the input impedance of the two circuits are identical.
b) The transistor amplifier shown in figure 1 uses a transistor with typical h parameter values. Calculate A_i, A_V, A_{Vs}, R_o and R_i. [5+5]

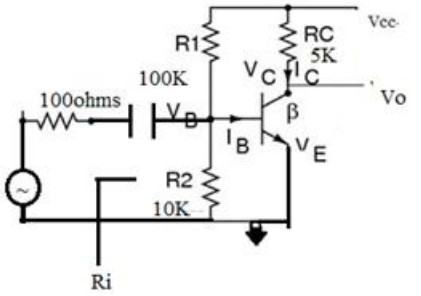

Figure: 1

OR

3.a) Draw the circuit diagram of Darlington emitter follower and derive the expression for input impedance.
b) Explain the working of cascade amplifier with neat circuit diagram. [5+5]

4.a) Draw the hybrid π equivalent circuit of a transistor in CE configuration and explain the various parameters in it.

b) A transistor biased at 5mA, 10V, h_{ie} =600Ω, h_{fe}=100, C_C=3pF and current gain of 10 at a frequency of 20MHz. Find β cut off frequency, gain band width product, C_e, $r_{b'e}$ and $r_{bb'}$ [5+5]

OR

5.a) Calculate the voltage gain of the FET amplifier shown in the figure 2. Assuming blocking capacitor to be large.g_m=4mA/V and r_d =5K.

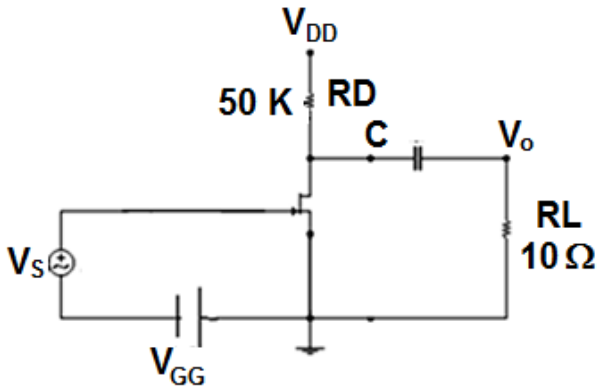

Figure: 2

b) Sketch the small signal model of a CD FET amplifier and derive equation for the voltage gain. [5+5]

6.a) Draw the negative feedback topologies and explain them.

b) An open loop amplifier has a midband gain of 500 and a pass band from 50Hz to 50KHz. Find voltage gain and cut off frequencies if 10% of output voltage is fed back. [5+5]

OR

7. Derive an expression for frequency of oscillations of a wien bridge oscillator using transistor. [10]

8.a) Explain how the efficiency of the class A power amplifier is improved by the transformer coupled amplifier configuration?

b) A transformer coupled class A power amplifier supplies the power to an 80Ω load connected across the secondary of a transformer having turns ration of 5:1. If I_c =120mA, find maximum output power? [6+4]

OR

9.a) Derive an equation of output power of a class B power amplifer.

b) Draw the circuit diagram of complementary symmetry class B pushpull amplifier and explain its working. [5+5]

10.a) Why is double tuning employed in tuned amplifier? What are the advantages of it?

b) What are applications of stagger tuned amplifier? [5+5]

OR

11.a) What are the high frequency limitations of a tuned amplifier? How are they eliminated?

b) How is the bandwidth of tuned amplifier improved? Draw such a circuit and explain its working. [5+5]

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Code No: 124CV **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, April - 2018
ELECTRONIC CIRCUIT ANALYSIS
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

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Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Draw the circuit diagram of Darlington Pair.	[2]
b)	What is the expression for harmonic distortion in single stage amplifiers?	[3]
c)	Define Gain-Bandwidth Product in detail.	[2]
d)	Draw the Small signal model of MOS amplifier.	[3]
e)	List out the Conditions for Oscillations in detail.	[2]
f)	Explain different Classification of Feedback Amplifiers.	[3]
g)	Define Thermal Stability and Thermal Runway.	[2]
h)	What is Heat sink and explain its advantages?	[3]
i)	Define Q factor.	[2]
j)	What is the expression for harmonic distortion in tuned amplifiers?	[3]

PART-B

(50 Marks)

2.a) Discuss about effect of Cb on frequency response of RC coupled amplifier.
b) Draw the circuit diagram of Direct Coupled Amplifier and explain its operation in detail. [5+5]

OR

3.a) With a neat circuit diagram. Explain about Boo-Strap emitter follower amplifier.
b) Derive the Analysis of CE amplifier with Emitter Resistance and explain its operation along with circuit diagram. [5+5]

4.a) Find the voltage gain, input and output resistances of a emitter follower at high Frequencies.
b) A common source amplifier uses a MOSFET with the following parameters gm=1.5mA/V, rd=40kohms, Cgs=3pF, Cds=1pF, Cgd=3.2pF. The value of Rd=200Kohms. The amplifier operates at 30KHz. Find Voltage gain, input resistance, output resistance and input capacitance. [5+5]

OR

5.a) Draw the circuit diagram of Common source amplifier with Resistive load and explain its operation.
b) Derive the expression for f_T of a transistor in detail. [5+5]

6.a) Derive the expression for frequency of oscillation of BJT RC phase-shift oscillator with necessary explanation.

b) What is the equivalent circuit of a crystal? Derive the expressions for series and parallel resonances. A crystal oscillator has the following parameters: L=0.33H, C=0.065pF, Cm=1.0pF and R=5.5 k ohm.
i) Find the series resonant frequency.
ii) Find the Q of the crystal. [5+5]

OR

7.a) Draw the block diagrams of four types of negative feedback amplifier circuits and explain the advantages and disadvantages with necessary derivations.

b) Explain why RC Phase shift oscillators are not used at high frequencies. [5+5]

8.a) Explain the operation of a class A push-pull power amplifier and list out its advantages and disadvantages.

b) A single transistor is operating as an ideal class B amplifier with a 10-K load. A dc meter in the collector circuit reads 8mA. How much signal power is delivered to the load? [5+5]

OR

9.a) Draw the circuit diagram of Complementary Symmetry Class B Push-Pull Amplifier and explain its operation.

b) List out the few difference between Class A, Class B and Class AB Push-Pull amplifiers with examples. [5+5]

10.a) What is a stagger tuned amplifier? Explain its advantages and disadvantages.

b) Write short notes on Small Signal Tuned Amplifiers in detail. [5+5]

OR

11.a) What are the different Effect of Cascading Single Tuned Amplifiers on Bandwidth in detail.

b) Explain the concept of Stability of Tuned Amplifiers with one example. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2017
ELECTRONIC CIRCUIT ANALYSIS
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

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PART- A

(25 Marks)

1.a) Draw a small signal low frequency model of a transistor. [2]
b) State dual of Miller's theorem and also write its applications. [3]
c) What is unity crossover frequency? [2]
d) Define a short circuit gain of a transistor in CE configuration at high frequencies. [3]
e) What is effect of negative feedback on amplifier gain? [2]
f) State Barkhausen criterion of oscillator. [3]
g) Why heat sinks are needed? [2]
h) What is mean by crossover distortion? [3]
i) Define Q factor of tuned amplifier. [2]
j) What are the limitations of Single tuned amplifier? [3]

PART-B

(50 Marks)

2.a) The h parameters of a transistor used in single stage amplifier circuit are h_{ic} = 1100, h_{rc} =1, h_{fc}==51 and h_{oc}=25μA. Determine the amplifier parameters for CC configuration when R_S=R_L=10K.
b) For any single-stage amplifier express input resistance in terms of current gain and h-parameters only. [5+5]

OR

3.a) Derive the bandwidth of a multistage amplifier, assuming that each stage has same upper and lower cut off frequencies.
b) For the two stage amplifier of the figure 1, calculate the input and output impedance, and the individual and overall voltage gains. Assume h_{fe} =50, h_{ie}=1.1kΩ, h_{re} = h_{oe}= 0. [5+5]

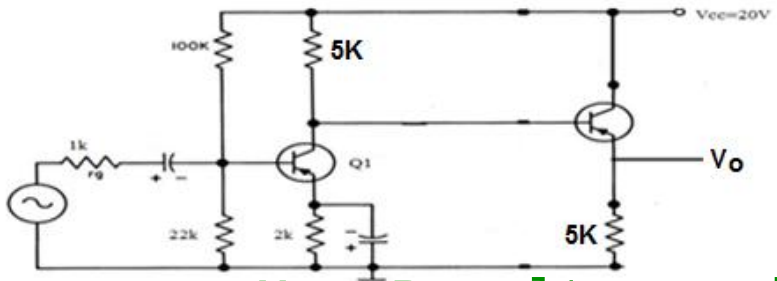

Figure: 1

4.a) A transistor biased at 20mA, 20V, it has the h-parameters at room temperature h_{ie} =500Ω, h_{fe}=100, h_{re} =10^{-4}, h_{oe} =4×10^{-5}℧. It has f_T =50MHz and C_C=3pF. Find all the values of hybrid π components.

b) The 3-db bandwidth of an amplifier extends from 20 Hz to 20 kHz. Find the frequency range over which the voltage gain differs by only 1 dB from the mid band value. [5+5]

OR

5.a) The amplifier of figure 2 uses a FET with I_{DSS} =3mA, V_p= -3V, r_d>>R_d. Find the quiescent drain current, quiescent drain to source voltage and A_V.

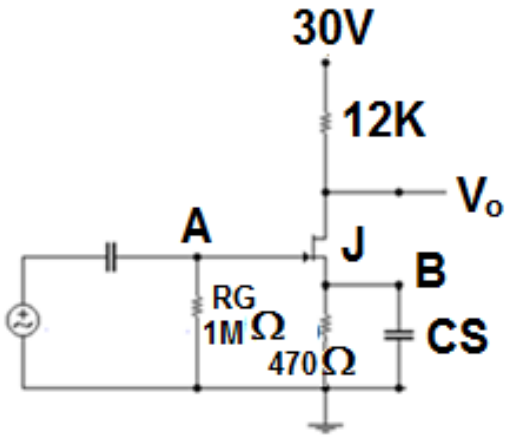

Figure: 2

b) Derive the equation for voltage gain of a CS FET amplifier. [5+5]

6.a) An amplifier has an open loop voltage gain of 1000 and delivers 10W output with 10% second harmonic distortion when the input is 10mV. Find the distortion of 60dB of negative feedback is applied.

b) Calculate A_{vf} = V_0/V_s, R_{if} and R_{of} for the circuit shown in figure 3 use typical h parameter values. Rs=R_C=10K and Re=1K. [5+5]

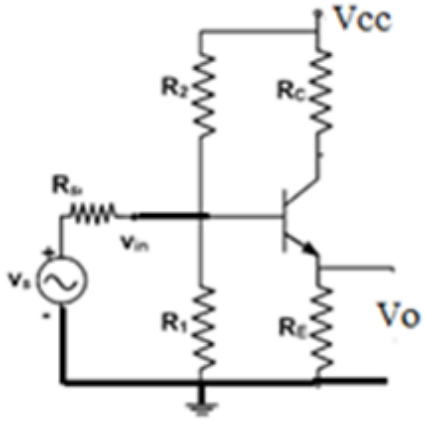

Figure: 3

OR

7.a) Derive an expression for frequency of oscillations of a RC phase shift oscillator using transistor.

b) A colpitts oscillator is designed with C_1 = 100pF and C_2=7500pF. Find the range of inductance values if the frequency of oscillations vary between 950 and 2050KHz. [5+5]

8.a) Classify amplifiers based on operating point selection. Compare them in terms of efficiency and distortion.

b) A transformer coupled class A large signal amplifier has maximum and minimum values of collector-to-emitter voltage of 25V and 2.5V. Determine its collector efficiency. [5+5]

OR

9.a) What is push pull configuration and how does this circuit reduce the harmonic distortion?

b) Given an ideal class B Push Pull amplifier whose collector supply voltage is V_{cc}, and $R_L' = n^2R_L$ are fixed as base current excitation is varied, show that the collector dissipation P_c is zero at no signal, rises as V_m increases and passes through a maximum at $V_m=2V_{cc}/\pi$. [5+5]

10. Draw the circuit diagram of double tuned amplifier and explain its working and derive the equation for bandwidth. [10]

OR

11.a) How to reduce the instability in tuned amplifier? Explain them with neat circuit diagram.

b) What are the advantages of stagger tuned amplifier? Draw its frequency response. [5+5]

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Code No: 124CV **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2017
ELECTRONIC CIRCUIT ANALYSIS
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

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Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **(25 Marks)**

1.a) Why is a CE amplifier widely used? List down its main limitations. [2]
b) What are the typical values of h-parameters of CE configuration? [3]
c) What is f_T of a BJT? [2]
d) State Miller's theorem. [3]
e) Compare Frequency stability of crystal oscillator, RC and LC oscillators. [2]
f) What are the advantages of negative feedback? [3]
g) What is Class-A power amplifier? [2]
h) Classify power Amplifiers. [3]
i) What is effect of cascading on single tuned amplifier? [2]
j) What is stagger tuned amplifier? [3]

PART-B **(50 Marks)**

2.a) Draw the CE amplifier with un bypassed emitter resistance and derive expression for R_i and A_v.
b) A transistor in CB circuit has the following set of 'h' parameters. h_{ib} = 20, h_{fb} = 0.98, $h_{rb} = 3\times10^{-4}$, $h_{ob} = 0.5\times10^{-6}$. Find the values if R_i, R_o, A_i and A_v, if $R_s = 600\Omega$ and $R_L = 1.5\ k\Omega$. [5+5]

OR

3.a) Draw the Darlington circuit and derive the expressions for the overall current gain, voltage gain, input impedance and output impedance.
b) With the help of a neat circuit diagram describe the working of a cascade amplifier. [5+5]

4.a) Draw the hybrid-Π model of common emitter configuration and describe each component in the Π-model.
b) Derive the equation for voltage gain bandwidth product for CE amplifier. [5+5]

OR

5.a) Discuss the effect of different types of loads to a common source MOS amplifier.
b) Draw the CS FET amplifier equivalent circuit looking into the drain and find its gain and output impedance. [5+5]

6.a) Explain the principle of negative feedback in amplifiers. Show quantitatively the effect of negative feedback on (i) Gain (ii) Stability (iii) Noise (iv) Distortion.

b) Show that current–series negative feedback increases the input impedance and increases the output impedance. [5+5]

OR

7. Starting from the description of a generalized Oscillator, derive the expression for frequency of Oscillation in a Colpitts Oscillator. [10]

8. Describe the operation of Class B Push pull amplifier and show how even harmonics are eliminated. [10]

OR

9.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.

b) A push pull amplifier utilizes a transformer whose primary has a total of 160 turns and whose secondary has 40 turns. It must be capable of delivering 40W to an 8 Ω load under maximum power conditions. What is the minimum possible value of V_{cc}? [5+5]

10. Explain the operation of doubled-tuned amplifier with a neat circuit diagram and derive the equation for its gain bandwidth product. [10]

OR

11. What is the effect of cascading double tuned Amplifiers on Band width? Derive the related equations. [10]

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Code No: 154AW **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, November/December - 2020
ELECTRONIC CIRCUIT ANALYSIS
(Common to ECE, EIE)

Time: 2 Hours **Max. Marks: 75**

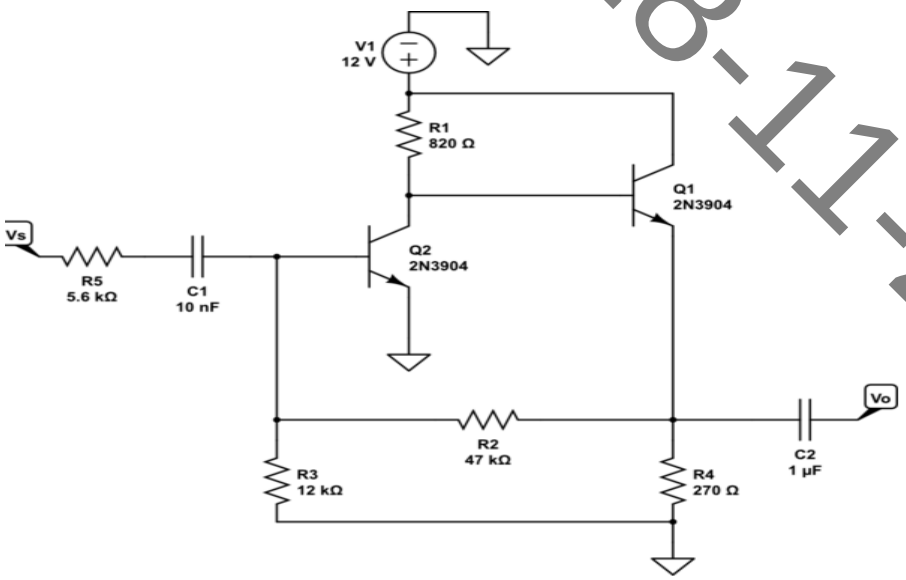
Answer any Five Questions
All Questions Carry Equal Marks
- - -

1.a) Derive the upper and lower cutoff frequencies of the common emitter amplifier.
b) Why 3dB frequency for the current gain is not same as the 3dB frequency for voltage gain? [9+6]

2.a) The bandwidth of a single stage amplifier extends from 10Hz to 100kHz. Find the frequencies at which the voltage gain is down by 1dB from its mid-band value.
b) Draw the circuit diagram of Darlington pair and explain how it provides high input impedance. [6+9]

3.a) A voltage amplifier is characterized by an open loop voltage gain of 100. Input resistance of 50KΩ and output resistance of 2KΩ, Negative feedback of 10% of output voltage is introduced in series with the input to bring the distortion below acceptable level. Find the modified values of these parameters.
b) Draw the current shunt feedback circuit diagram. [8+7]

4. Determine the feedback factor, current gain, voltage gain, input and output impedances for the following circuit. Assume ideal h parameters for the transistors. [15]



5. Derive the expression for the phase shift as a function of frequency for the feedback network of RC phase shift oscillator. [15]

6.a) How does the frequency stability of an LC oscillator depend upon the Q-factor of the LC circuit? Explain.

b) Determine the minimum amplifier gain and the phase shift required to be introduced by the amplifier for the following case: Feedback factor =2%, oscillator type is Hartley oscillator. [8+7]

7.a) A class B amplifier provides a 15V peak output signal to 10Ω load. The system operates on a power supply of 20V. Determine the efficiency of the amplifier.

b) Draw the circuit diagram of push-pull class-B power amplifier and explain its working. [7+8]

8.a) Define the terms slope error, displacement error, transmission error.

b) With the help of circuit diagram explain the principle of operation of a constant current sweep circuit. [7+8]

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